

100V, 175A, 3.2mΩ N-channel Power SGT MOSFET

JBE113P

Features

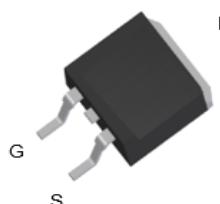
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% ΔV_{ds} Tested
- Halogen-free; RoHS-compliant

Product Summary

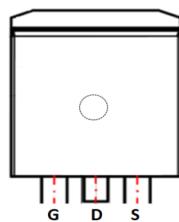
Parameters	Value	Unit
V_{DSS}	100	V
$V_{GS(th)}_{Typ}$	2.9	V
$I_D(@V_{GS}=10V)$	175	A
$R_{DS(ON)}_{Typ}(@V_{GS}=10V)$	3.2	mΩ

Applications

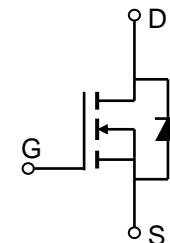
- Load Switch
- PWM Application
- Power Management



TO-263-3L



Pin Assignment



Schematic Diagram

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
JBE113P	BE113P	3	Tape&Reel	TO-263-3L	800	4000

Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$	175
		$T_C = 100^\circ\text{C}$	111
I_{DM}	Pulsed Drain Current ⁽¹⁾	Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	953	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	250
		$T_C = 100^\circ\text{C}$	100
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	33	°C/W
	Thermal Resistance, Junction to Case	0.5	

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.0	2.9	4.1	V
$R_{\text{DS(ON)}}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}, I_D = 20\text{A}$	-	3.2	4.1	$\text{m}\Omega$
Dynamic Characteristics						
R_g	Gate Resistance	$f = 1\text{MHz}$	-	2.1	-	Ω
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 50\text{V}, f = 1\text{MHz}$	4387	6142	8292	pF
C_{oss}	Output Capacitance		766	1073	1448	pF
C_{rss}	Reverse Transfer Capacitance		19	27	36	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 50\text{V}, I_D = 20\text{A}$	63	88	118	nC
Q_{gs}	Gate Source Charge		22	31	41	nC
Q_{gd}	Gate Drain("Miller") Charge		13	18	25	nC
Switching Characteristics						
$t_{d(\text{on})}$	Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DD} = 50\text{V}$ $I_D = 20\text{A}, R_{\text{GEN}} = 6.2\Omega$	-	29	-	ns
t_r	Turn-On Rise Time		-	41	-	ns
$t_{d(\text{off})}$	Turn-Off Delay Time		-	69	-	ns
t_f	Turn-Off Fall Time		-	44	-	ns
Body Diode Characteristics						
I_S	Maximum Continuous Body Diode Forward Current	-	-	175	-	A
I_{SM}	Maximum Pulsed Body Diode Forward Current	-	-	699	-	A
V_{SD}	Body Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 20\text{A}$	-		1.2	V
trr	Body Diode Reverse Recovery Time	$I_F = 20\text{A}, di/dt = 100\text{A/us}$	60	84	113	ns
Qrr	Body Diode Reverse Recovery Charge		-	240	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=50\text{V}$, $V_G=10\text{V}$, $R_G=25\text{ohm}$, $L=3\text{mH}$, $I_{AS}=25.2\text{A}$, $V_{DD}=0\text{V}$ during time in avalanche.
 3. $R_{\theta JA}$ is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB.
 4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.



Typical Performance Characteristics

Figure 1: Power De-rating

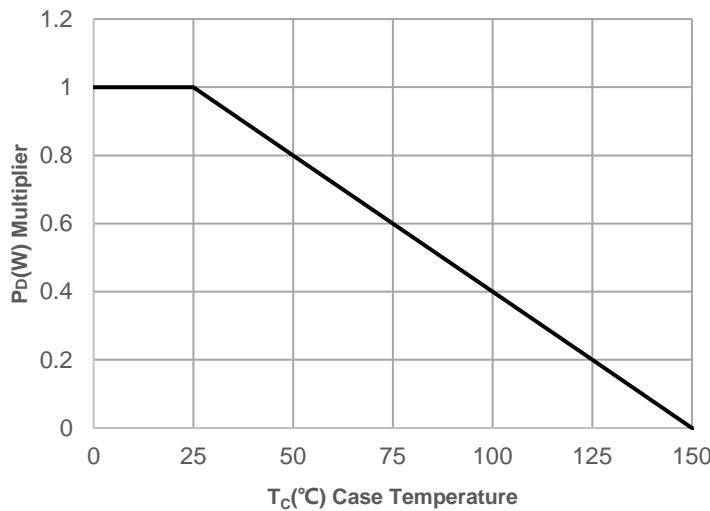


Figure 2: Current De-rating

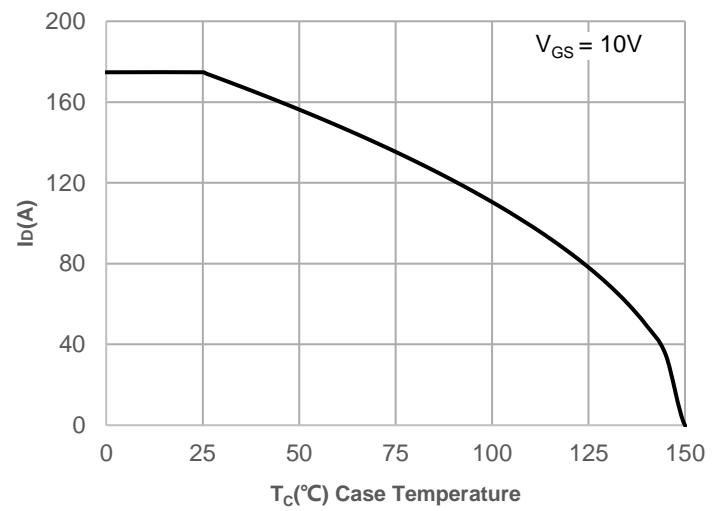


Figure 3: Normalized Maximum Transient Thermal Impedance

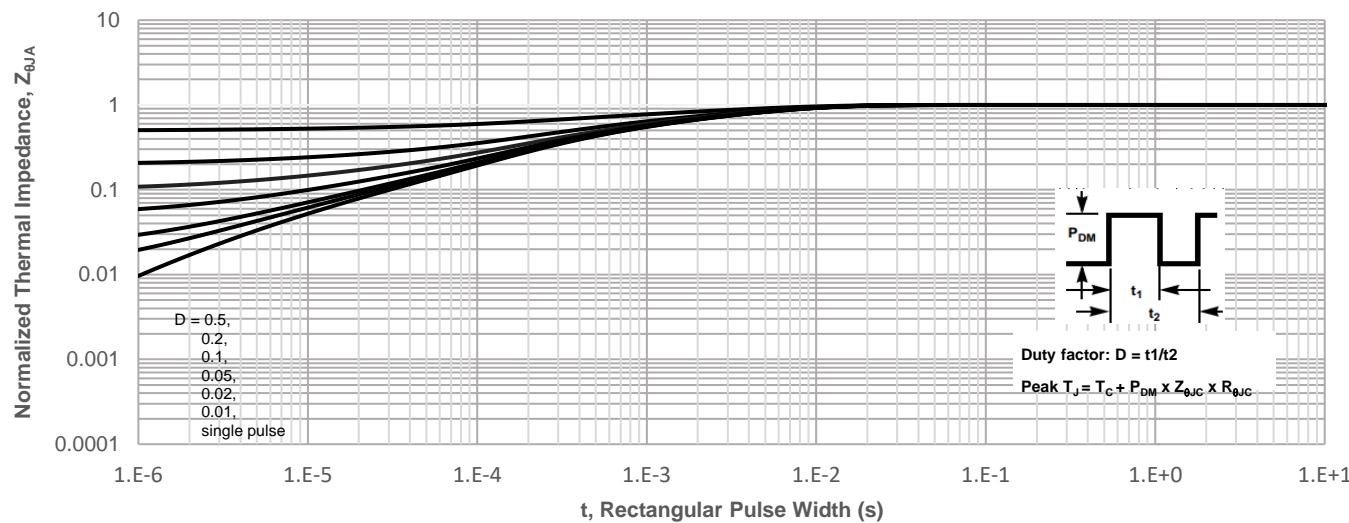
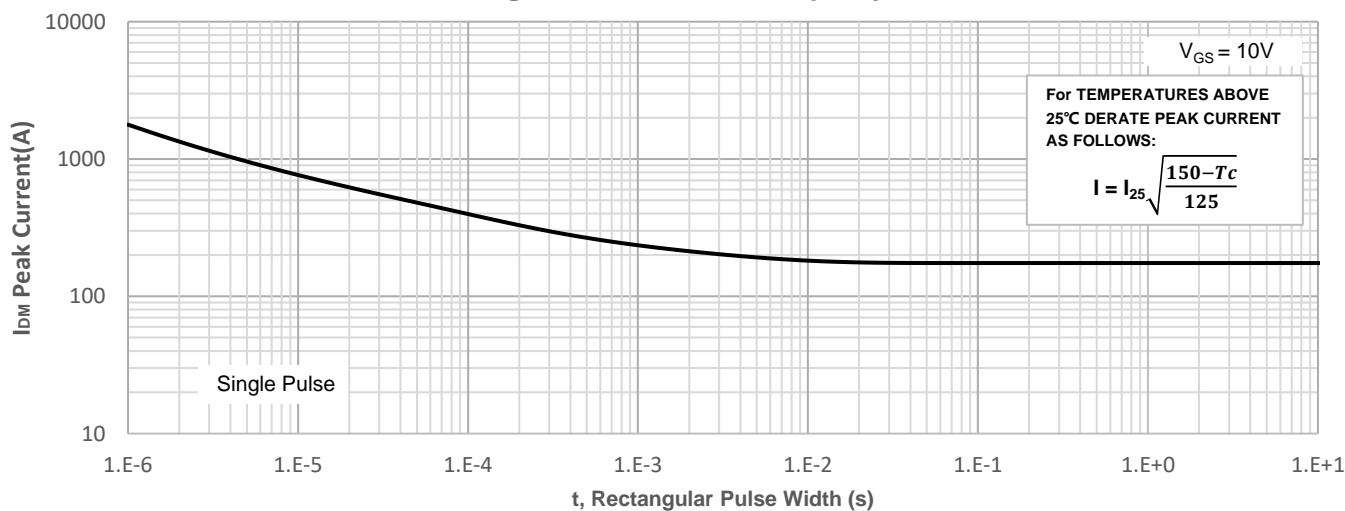


Figure 4: Peak Current Capacity



Typical Performance Characteristics

Figure 5: Output Characteristics

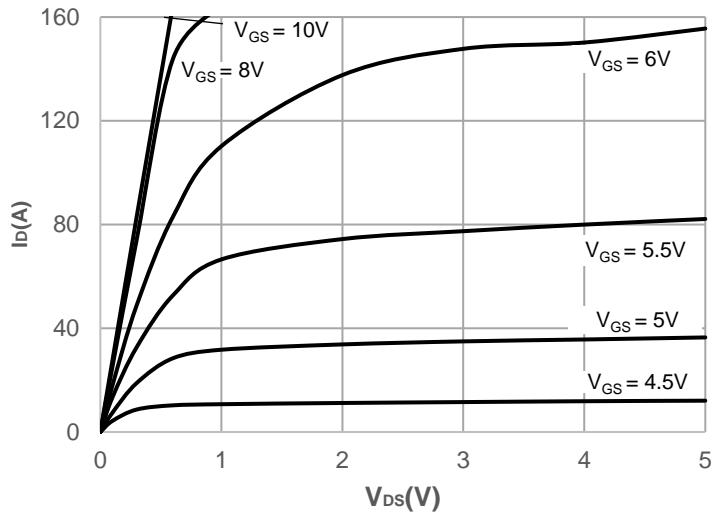


Figure 6: Typical Transfer Characteristics

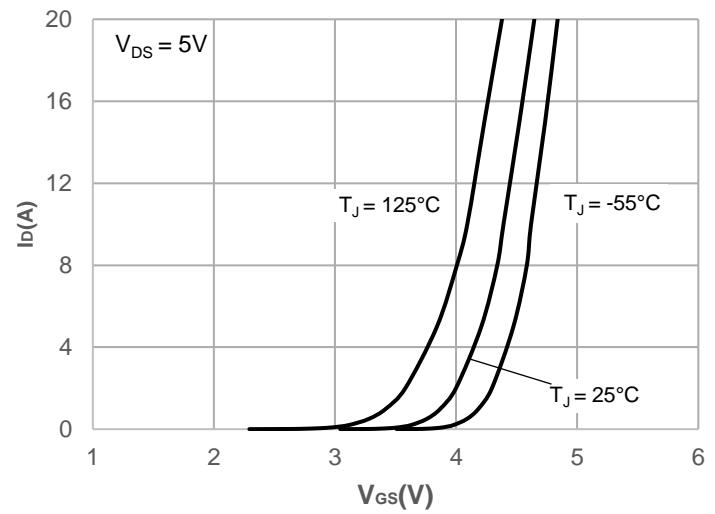


Figure 7: On-resistance vs. Drain Current

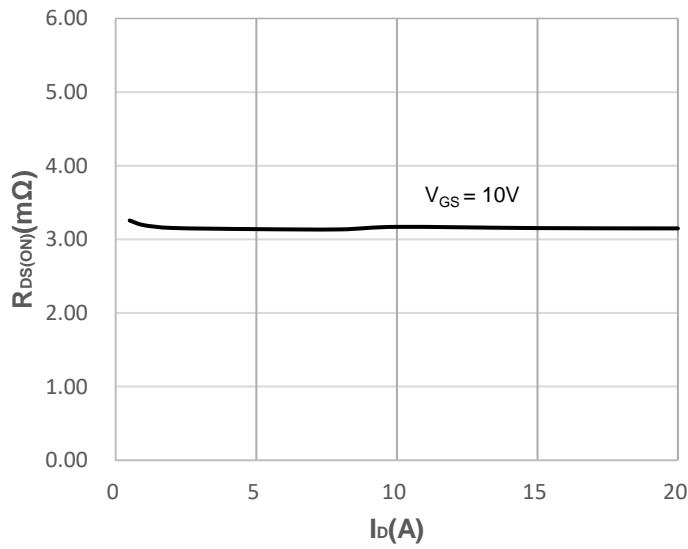


Figure 8: Body Diode Characteristics

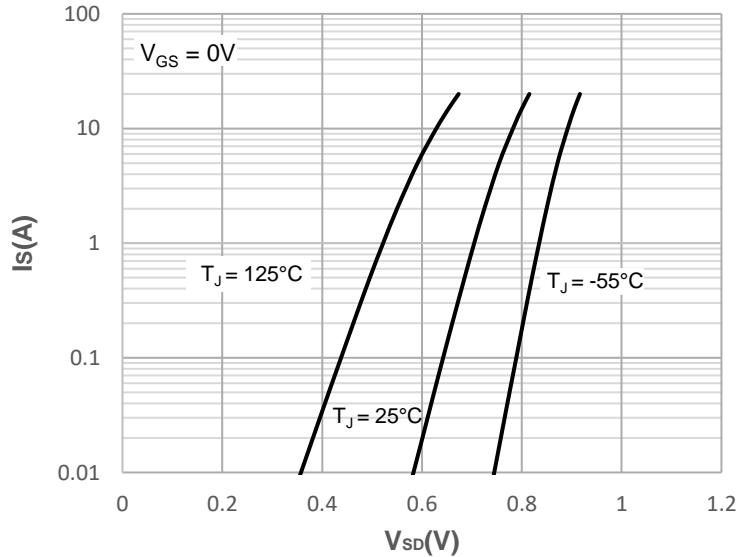


Figure 9: Gate Charge Characteristics

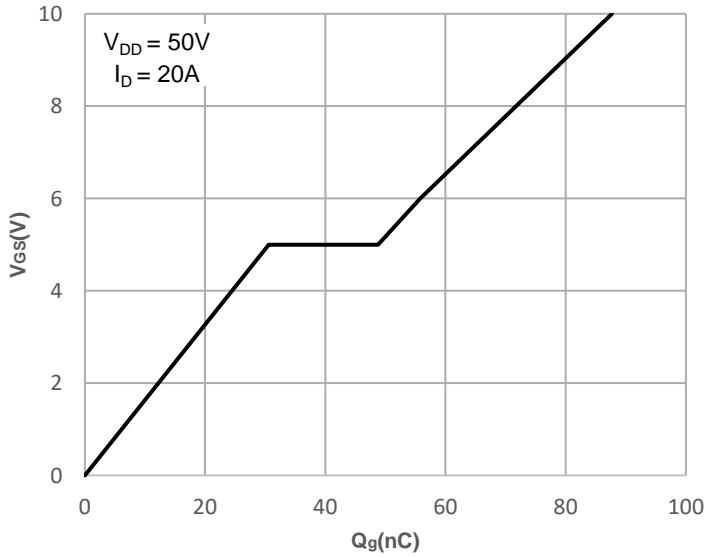
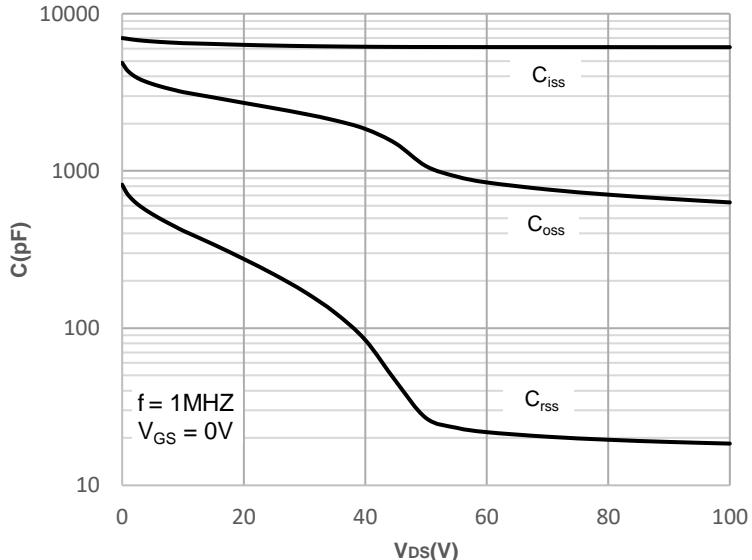


Figure 10: Capacitance Characteristics



Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

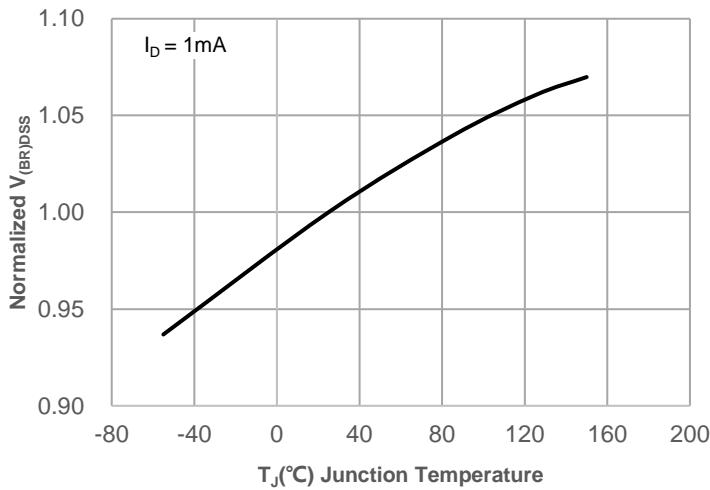


Figure 12: Normalized on Resistance vs. Junction Temperature

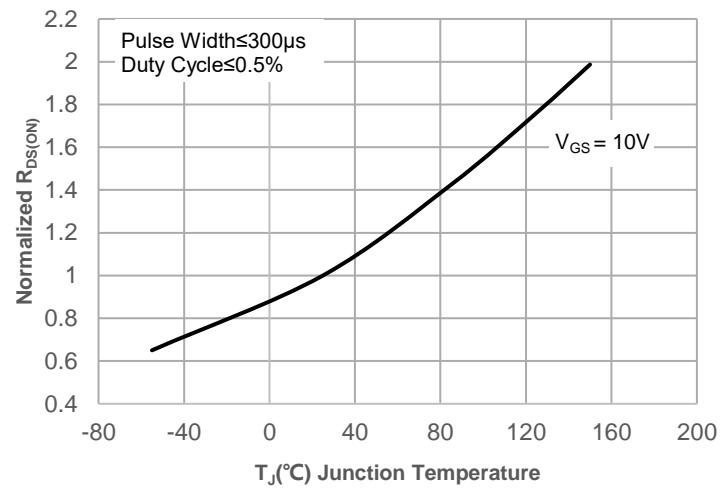


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

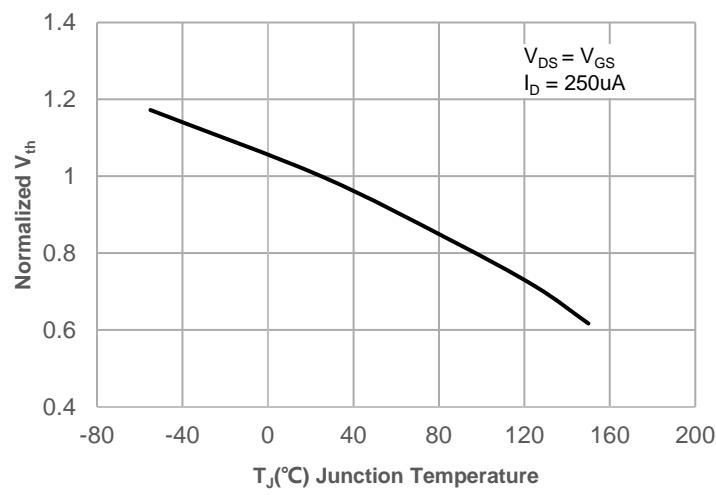


Figure 14: R_{D_{S(ON)}} vs. V_{GS}

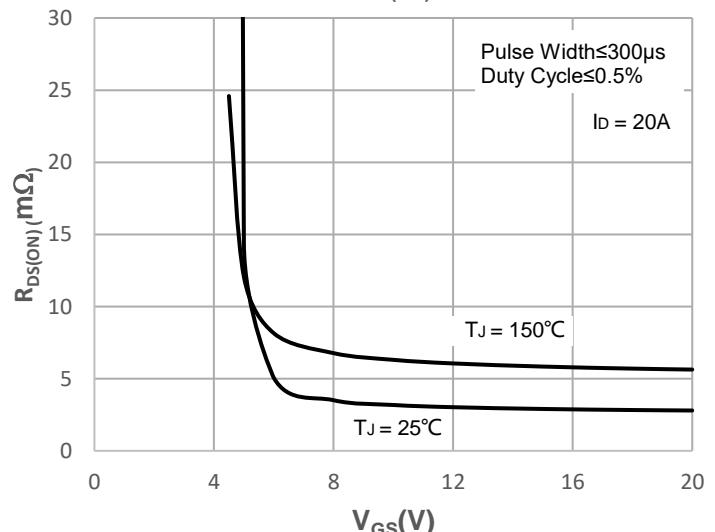
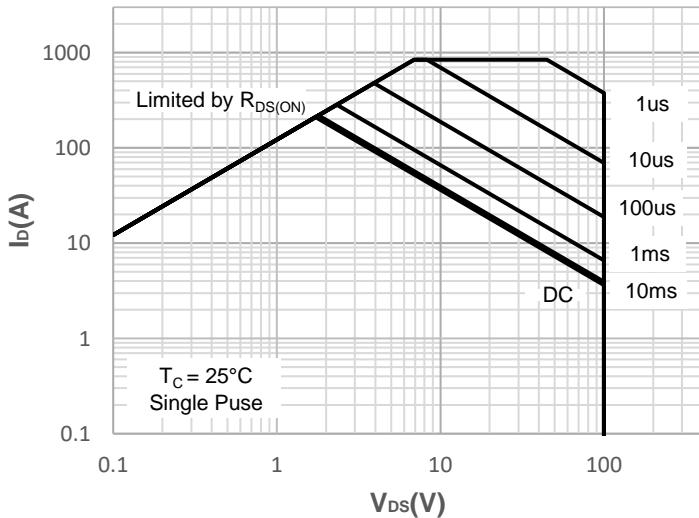


Figure 15: Maximum Safe Operating Area



Test Circuit

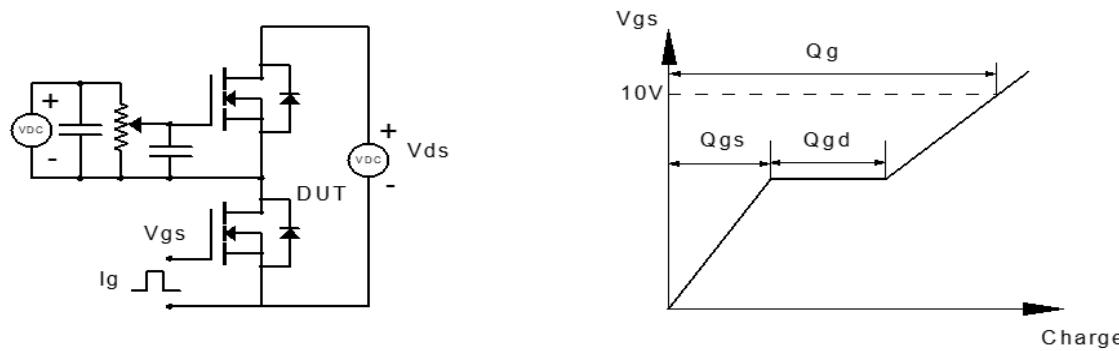


Figure 1: Gate Charge Test Circuit & Waveform

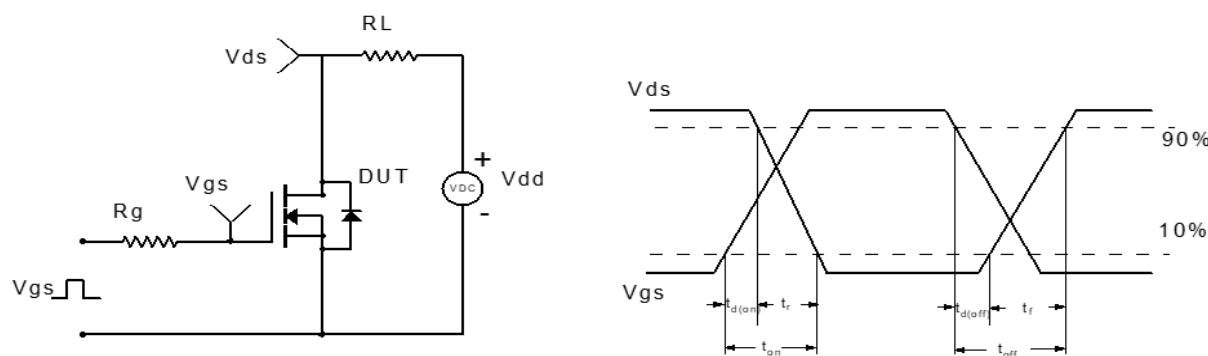


Figure 2: Resistive Switching Test Circuit & Waveform

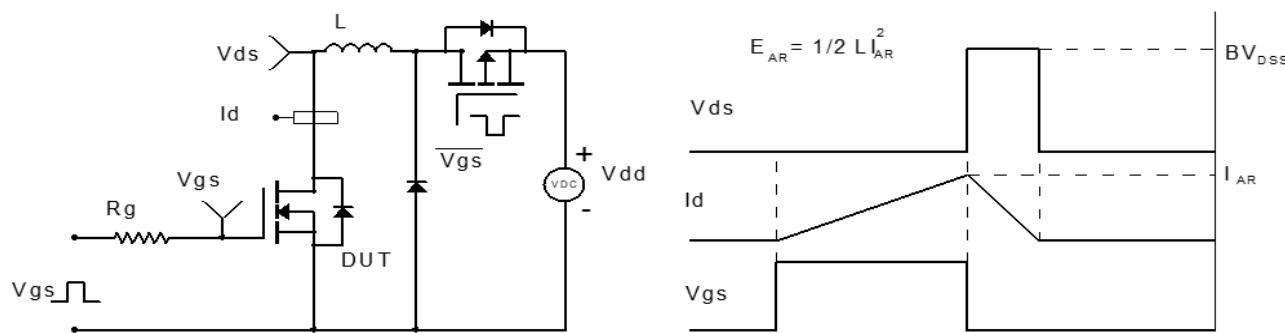


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

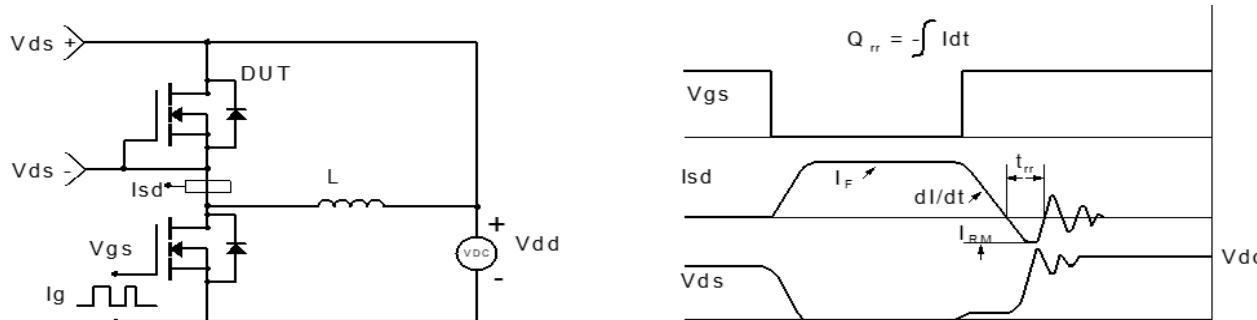
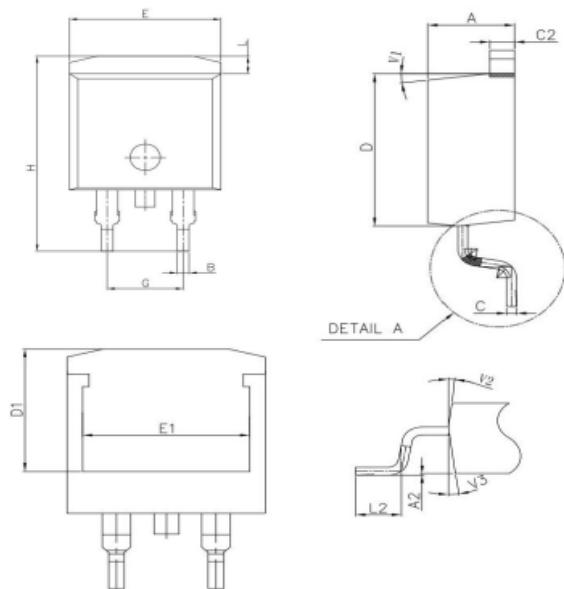


Figure 4: Diode Recovery Test Circuit & Waveform



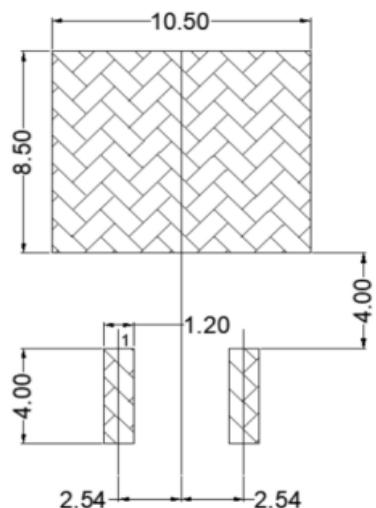
Package Mechanical Data(TO-263-3L)

Package Outline



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	4.3	4.55	4.7
A2	0		0.25
B	0.75	0.8	0.85
C	0.38	0.46	0.55
C2	1.25	1.3	1.35
D	8.9	9.3	9.6
D1	7.4	7.65	7.9
E	9.9	10.05	10.21
E1	8.3	8.6	8.9
G	5.03	5.08	5.13
H	14.7	15	15.8
L2	2.2	2.35	2.5

Recommended Footprint



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